**4:1 Mux using Behavioral modeling**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity Mux\_4\_1 is

Port ( a,b,c,d : in STD\_LOGIC;

s : in STD\_LOGIC\_VECTOR (1 downto 0);

y : out STD\_LOGIC);

end Mux\_4\_1;

architecture Behavioral of Mux\_4\_1 is

begin

process (a,b,c,d,s) is

begin

if (s="00") then

y <= a;

elsif (s="01") then

y <= b;

elsif (s="10") then

y <= c;

else

y <= d;

end if;

end process;

end Behavioral;



